

CLAIMS:

What is claimed is:

1. An apparatus comprising:
 - a processor handling an I/O request in an I/O operation;
 - main storage controlled by the processor for storing data;
 - one or more I/O devices for sending data to or receiving data from said main storage;
 - a vector mechanism operable to register I/O requests by said devices to send or receive data from said main storage;
 - a dispatcher operable to poll said vector mechanism to determine if there is an outstanding I/O request; and
 - an override bit having a first condition when an immediate interrupt is to be sent to said processor for handling an I/O request from said I/O device(s), and a second condition when said dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said override bit being set to its first condition or reset to its second condition by said processor.
2. The apparatus of claim 1 further comprising a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first condition, overrides said TDI value and drives an immediate interrupt to said processor.
3. The apparatus of claim 1 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor for setting the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

1 4. The apparatus of claim 3 further comprising one or more central processing units (CPUs)
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 5. The apparatus of claim 1 wherein said override bit is reset to its second condition after an
2 interrupt is handled by said processor.

1 6. The apparatus of claim 5 wherein said override bit is reset to its second condition after said
2 dispatcher polls said vector mechanism, said resetting of said override bit to its second condition
3 upon the first to occur of said interrupt handling or said dispatcher polling.

1 7. An apparatus controlling the transfer of data in a data processing system having a
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main
4 storage, said apparatus comprising:

5 a vector mechanism operable to register I/O requests by said devices to send or receive
6 data from said main storage;

7 a dispatcher operable to poll said vector mechanism to determine if there is an outstanding
8 I/O request;

9 an override bit having a first condition when an immediate interrupt is to be sent to said
10 processor for handling an I/O request from said I/O device(s), and a second condition when said
11 dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said
12 override bit being set to its first condition or reset to its second condition by said processor.

1 8. The apparatus of claim 7 further comprising a Target Delay Interval (TDI) register
2 containing a TDI value for determining when the vector mechanism should not be polled by said
3 dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first
4 condition, overrides said TDI value and drives an immediate interrupt to said processor.

1 9. The apparatus of claim 7 wherein said main storage is divided into multiple partitions, with
2 each partition having a vector mechanism operable to register I/O requests by said devices to send
3 or receive data from that partition of main storage, each partition having an associated override bit
4 for that partition, and said processor is a hypervisor for setting the override bit for that partition
5 when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for
6 that partition.

1 10. The apparatus of claim 9 further comprising one or more central processing units (CPUs)
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 11. The apparatus of claim 7 wherein said override bit is reset to its second condition after an
2 interrupt is handled by said processor.

1 12. The apparatus of claim 11 wherein said override bit is reset to its second condition after
2 said dispatcher polls said vector mechanism, said resetting of said override bit to its second
3 condition upon the first to occur of said interrupt handling or said dispatcher polling.

1 13. A method for controlling the transfer of data in a data processing system having a
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main
4 storage, said method comprising:
5 registering in a vector mechanism, I/O requests by said devices to send or receive data
6 from said main storage;
7 polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O
8 request; and
9 sending an immediate interrupt to said processor when an override bit has a first condition
10 for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector
11 mechanism to determine if there is an outstanding I/O request when said override bit is in a second
12 condition.

1 14. The method of claim 13 wherein said data processing further includes a Target Delay
2 Interval (TDI) register containing a TDI value for determining when the vector mechanism should
3 not be polled by said dispatcher and an interrupt given to said processor, said method further
4 comprising overriding said TDI value and driving an immediate interrupt to said processor when
5 said override bit is in its first condition.

1 15. The method of claim 13 wherein said main storage is divided into multiple partitions, with
2 each partition having a vector mechanism operable to register I/O requests by said devices to send
3 or receive data from that partition of main storage, each partition having an associated override bit
4 for that partition, and said processor is a hypervisor, said method further comprising setting by said
5 hypervisor the override bit for that partition when said hypervisor is to handle an immediate
6 interrupt rather than polling by said dispatcher for that partition.

1 16. The method of claim 15 wherein said data processing system further includes one or more
2 central processing units (CPUs) assignable by said hypervisor to one or more of said partitions,
3 said method further comprising setting by said hypervisor, the override bit of one partition when
4 that partition does not have a CPU assigned to it.

1 17. The method of claim 13 further comprising resetting said override bit to its second
2 condition after an interrupt is handled by said processor.

1 18. The method of claim 17 further comprising resetting said override bit to its second
2 condition upon the first to occur for said interrupt handling or said dispatcher polling.

1 19. A program product for controlling the transfer of data in a data processing system having
2 a processor handling an I/O request in an I/O operation, main storage controlled by the processor
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main
4 storage, said program product comprising:

5 a computer readable medium having recorded thereon computer readable program code
6 means for performing the method comprising:

7 registering in a vector mechanism, I/O requests by said devices to send or receive data
8 from said main storage;
9 polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O
10 request; and
11 sending an immediate interrupt to said processor when an override bit has a first condition
12 for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector
13 mechanism to determine if there is an outstanding I/O request when said override bit is in a second
14 condition..

1 20. The program product of claim 19 wherein said data processing further includes a Target
2 Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism
3 should not be polled by said dispatcher and an interrupt given to said processor, said method
4 further comprising overriding said TDI value and driving an immediate interrupt to said processor
5 when said override bit is in its first condition.

1 21. The program product of claim 19 wherein said main storage is divided into multiple
2 partitions, with each partition having a vector mechanism operable to register I/O requests by said
3 devices to send or receive data from that partition of main storage, each partition having an
4 associated override bit for that partition, and said processor is a hypervisor, said method further
5 comprising setting by said hypervisor the override bit for that partition when said hypervisor is to
6 handle an immediate interrupt rather than polling by said dispatcher for that partition.

1 22. The program product of claim 21 wherein said data processing system further includes one
2 or more central processing units (CPUs) assignable by said hypervisor to one or more of said
3 partitions, said method further comprising setting by said hypervisor, the override bit of one
4 partition when that partition does not have a CPU assigned to it.

1 23. The program product of claim 19 wherein said method further comprises resetting said
2 override bit to its second condition after an interrupt is handled by said processor.



g0014	g10012	g10013	g10014	g10015	g10016	g10017	g10018	g10019	g10020	g10021	g10022	g10023	g10024	g10025	g10026	g10027	g10028	g10029	g10030	g10031	g10032	g10033	g10034	g10035	g10036	g10037	g10038	g10039	g10040	g10041	g10042	g10043	g10044	g10045	g10046	g10047	g10048	g10049	g10050	g10051	g10052	g10053	g10054	g10055	g10056	g10057	g10058	g10059	g10060	g10061	g10062	g10063	g10064	g10065	g10066	g10067	g10068	g10069	g10070	g10071	g10072	g10073	g10074	g10075	g10076	g10077	g10078	g10079	g10080	g10081	g10082	g10083	g10084	g10085	g10086	g10087	g10088	g10089	g10090	g10091	g10092	g10093	g10094	g10095	g10096	g10097	g10098	g10099	g10100	g10101	g10102	g10103	g10104	g10105	g10106	g10107	g10108	g10109	g10110	g10111	g10112	g10113	g10114	g10115	g10116	g10117	g10118	g10119	g10120	g10121	g10122	g10123	g10124	g10125	g10126	g10127	g10128	g10129	g10130	g10131	g10132	g10133	g10134	g10135	g10136	g10137	g10138	g10139	g10140	g10141	g10142	g10143	g10144	g10145	g10146	g10147	g10148	g10149	g10150	g10151	g10152	g10153	g10154	g10155	g10156	g10157	g10158	g10159	g10160	g10161	g10162	g10163	g10164	g10165	g10166	g10167	g10168	g10169	g10170	g10171	g10172	g10173	g10174	g10175	g10176	g10177	g10178	g10179	g10180	g10181	g10182	g10183	g10184	g10185	g10186	g10187	g10188	g10189	g10190	g10191	g10192	g10193	g10194	g10195	g10196	g10197	g10198	g10199	g10200	g10201	g10202	g10203	g10204	g10205	g10206	g10207	g10208	g10209	g10210	g10211	g10212	g10213	g10214	g10215	g10216	g10217	g10218	g10219	g10220	g10221	g10222	g10223	g10224	g10225	g10226	g10227	g10228	g10229	g10230	g10231	g10232	g10233	g10234	g10235	g10236	g10237	g10238	g10239	g10240	g10241	g10242	g10243	g10244	g10245	g10246	g10247	g10248	g10249	g10250	g10251	g10252	g10253	g10254	g10255	g10256	g10257	g10258	g10259	g10260	g10261	g10262	g10263	g10264	g10265	g10266	g10267	g10268	g10269	g10270	g10271	g10272	g10273	g10274	g10275	g10276	g10277	g10278	g10279	g10280	g10281	g10282	g10283	g10284	g10285	g10286	g10287	g10288	g10289	g10290	g10291	g10292	g10293	g10294	g10295	g10296	g10297	g10298	g10299	g10300	g10301	g10302	g10303	g10304	g10305	g10306	g10307	g10308	g10309	g10310	g10311	g10312	g10313	g10314	g10315	g10316	g10317	g10318	g10319	g10320	g10321	g10322	g10323	g10324	g10325	g10326	g10327	g10328	g10329	g10330	g10331	g10332	g10333	g10334	g10335	g10336	g10337	g10338	g10339	g10340	g10341	g10342	g10343	g10344	g10345	g10346	g10347	g10348	g10349	g10350	g10351	g10352	g10353	g10354	g10355	g10356	g10357	g10358	g10359	g10360	g10361	g10362	g10363	g10364	g10365	g10366	g10367	g10368	g10369	g10370	g10371	g10372	g10373	g10374	g10375	g10376	g10377	g10378	g10379	g10380	g10381	g1038
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